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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,315	01/23/2004	Shinya Ito	17381	7794

23389 7590 04/26/2007

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EXAMINER	
SARKAR, ASOK K	
ART UNIT	**PAPER NUMBER**
2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,315	ITO, SHINYA	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *9-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 15-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 5, 2007 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: In line 9, after the word and step (e) should be inserted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 – 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, US 6,468,904 in view of Wang, US 6,448,167 and Lee, US 6,518,136.

Regarding claim 1, Chen teaches a method of fabricating a semiconductor device, comprising in sequence:

- (a) forming an oxide film 20 entirely over a semiconductor substrate 10 on which a MOS transistor is fabricated (see Fig. 2);
- (b) selectively removing said oxide film in an area where later mentioned semiconductor – metal compound is to be formed while leaving oxide film in a non – silicide transistor region (see Fig. 3 and 5 and in column 3, lines 5 – 28);
- (d) forming a metal film entirely over said semiconductor substrate (column 3, lines 29 – 31); and
- (e) carrying out second thermal – annealing to said semiconductor substrate to form semiconductor – metal compound in said area (see Fig. 6, column 3, lines 29 – 31).

Chen teaches forming the source and drains with reference to Fig. 1, but fails to teach the step (b) carrying out spike thermal annealing (RTA) as first thermal – annealing to said semiconductor substrate.

Wang teaches a method of forming a MOSFET in which he uses the RPO oxide layer, which is similar to that of Chen and in the same field of endeavor in

which he teaches the steps of implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions; and carrying out first thermal – annealing to said semiconductor substrate in column 5, lines 4 – 21 for the benefit of protecting the underlying MOSFET elements during the activation annealing cycle in column 5, lines 5 – 8.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and carry out the steps of implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions; and carrying out first thermal – annealing to said semiconductor substrate for the benefit of protecting the underlying MOSFET elements during the activation annealing cycle as taught by Wang in column 5, lines 5 – 8.

Wang fails to teach the spike RTA as the annealing step for activating the dopants.

Lee teaches spike thermal annealing for activating all implanted dopants which is similar to that of Chen and in the same field of endeavor in column 4, lines 14 – 23 for the benefit of providing a much reduced thermal cycle due to rapid thermal anneal cycle in column 4, lines 32 – 36.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and carry out the step or RTA as a spike anneal for the benefit of providing a much reduced thermal cycle due to rapid thermal anneal cycle as taught by Lee in column 4, lines 32 – 36.

Regarding claim 2, Chen teaches removing said metal film having been

not reacted with said semiconductor substrate in column 3, lines 33 – 35.

Regarding claim 3, Chen teaches silicon substrate in column 2, lines 29 – 31 and the semiconductor – metal compound as silicide in column 3, line 33.

Regarding claim 4, Chen teaches metal film as cobalt in column 3, line 32.

Regarding claim 5, Chen teaches the oxide film is formed by chemical vapor deposition (CVD) by the thickness of 20 to 40 nanometers in column 2, lines 60 – 63 but fails to teach the temperature range of 300 to 500 degrees centigrade both inclusive.

Wang teaches the oxide film is formed by chemical vapor deposition (CVD) in the range of 300 to 500 degrees centigrade both inclusive for the benefit of forming the oxide layer from precursor gases by the CVD process in column 5, lines 4 – 14.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and deposit the silicon oxide in the temperature range of 300 to 500 degrees centigrade both inclusive for the benefit of forming the oxide layer from precursor gases by the CVD process as taught by Wang in column 5, lines 4 – 14.

Regarding claim 6, Chen fails to teach RTA for the first thermal annealing.

Wang teaches the first thermal – annealing is carried out as spike rapid thermal annealing (RTA) by zero second in the range of 1000 to 1100 degrees centigrade for the benefit of activating the implanted ions in column 5, lines 13 – 17.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and carry out the first thermal – annealing as spike rapid thermal annealing (RTA) by zero second in the range of 1000 to 1100 degrees centigrade for the benefit of activating the implanted ions as taught by Wang in column 5, lines 13 – 17.

Regarding claim 7, Chen fails to teach the first thermal annealing for activating the implanted ions into source and drain.

Wang teaches the first thermal – annealing is carried out also for the benefit of activating impurities having been implanted into source and drain regions of said MOS transistor, and for removing defects in said source and drain regions in column 5, lines 4 – 14.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and carry out first thermal – annealing for the benefit of activating impurities having been implanted into source and drain regions of said MOS transistor, and for removing defects in said source and drain regions as taught by Wang in column 5, lines 4 – 14.

Regarding claims 8 and 15, Chen teaches shallow trench isolation with oxide in trench (STI) film with reference to Fig. 1 in column 2, lines 28 – 36.

6. Claims 16 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, US 6,468,904 in view of Wang, US 6,448,167.

Regarding claim 16, Chen teaches a method of fabricating a semiconductor device, comprising, in sequence:

(a) forming a shallow trench isolation (STI) film on a semiconductor substrate;

(c) forming an oxide film entirely over said semiconductor substrate on which a MOS transistor is fabricated;

(e) selectively removing said oxide film in an area where later mentioned semiconductor – metal compound is to be formed while leaving said oxide film in a non – silicide transistor region;

(f) forming a metal film entirely over said semiconductor substrate; and

(g) carrying out second thermal – annealing to said semiconductor substrate to form semiconductor – metal compound in said area as was described earlier in rejecting claim 1.

Chen fails to teach the steps

(b) implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions;

d) carrying out first thermal-annealing to said semiconductor substrate:

wherein no thermal – annealing steps are carried out between said (b) and (c) so as to prevent a recess at a shoulder of said shallow trench isolation film from deepening.

Wang teaches a method of forming a MOSFET in which he uses the RPO oxide layer, which is similar to that of Chen and in the same field of endeavor in which he teaches the steps of implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions; and carrying out first thermal-annealing to said semiconductor substrate

wherein no thermal – annealing steps are carried out between the two steps in column 5, lines 4 – 21 for the benefit of protecting the underlying MOSFET elements during the activation annealing cycle in column 5, lines 5 – 8.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chen and carry out the steps of implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions; and carrying out first thermal-annealing to said semiconductor substrate wherein no thermal – annealing steps are carried out between the two steps for the benefit of protecting the underlying MOSFET elements during the activation annealing cycle as taught by Wang in column 5, lines 5 – 8.

Wang fails to teach that the first annealing step is done as to prevent a recess at a shoulder of said shallow trench isolation film from deepening. However, it will be obvious in the process since the STI are formed early in the process.

Regarding claims 17 – 22, the limitations have been described earlier in rejecting claims 2 – 7.

Response to Arguments

7. Applicant's arguments filed February 2, 2007 have been fully considered but they are not persuasive.

The Applicant's first argument with respect to claims 1 – 8 and 15 in page 7 is moot in view of the new rejection as described above in detail.

The Applicant's second argument deals with claims 16 – 22 (see

pages 7 and 8) in which he alleges that combining teachings of Chen with wang will not provide the silicide block in the non – silicided region as recited in claim 16 par (e). In response to applicant's argument against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As mentioned earlier in the rejection, Chen teaches all steps of claim 16 except (b) and (d). Wang was therefore used for teaching these two steps wherein no thermal - annealing steps are carried out between the two steps for the benefit of protecting the underlying MOSFET elements during the activation annealing cycle. The Applicant seems to have included various extra steps in their argument in page 8. The arguments were not persuasive. Since the limitations of the claim 16 is taught by Chen in view of Wang it will be obvious that no deep recess will form at a shoulder of the shallow trench isolation film.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Asok K. Sarkar
April 24, 2007

Primary Examiner